L Number	Hits	Search Text	DB	Time stamp
1	2844187	memory or storage	USPAT;	2004/07/07 18:07
			US-PGPUB;	
			EPO; JPO;	
			DERWENT	
2	206	(memory or storage) and (sram or static) with compatible	USPAT;	2004/07/07 18:08
		with (dram or dynamic)	US-PGPUB;	
			EPO; JPO;	
			DERWENT	
3	9	((memory or storage) and (sram or static) with compatible	USPAT;	2004/07/07 18:09
		with (dram or dynamic)) and control\$6 with (dynamic or	US-PGPUB;	
		dram) with chip adj2 enabl\$6	EPO; JPO;	
			DERWENT	
4	7	(((memory or storage) and (sram or static) with compatible	USPAT;	2004/07/07 18:10
		with (dram or dynamic)) and control\$6 with (dynamic or	US-PGPUB;	
		dram) with chip adj2 enabl\$6) and refresh\$5	EPO; JPO;	
	_		DERWENT	
5	7	((((memory or storage) and (sram or static) with compatible	USPAT;	2004/07/07 18:10
		with (dram or dynamic)) and control\$6 with (dynamic or	US-PGPUB;	-
		dram) with chip adj2 enabl\$6) and refresh\$5) and clock	EPO; JPO;	
			DERWENT	
6	4	(((((memory or storage) and (sram or static) with	USPAT;	2004/07/07 18:13
		compatible with (dram or dynamic)) and control\$6 with	US-PGPUB;	
		(dynamic or dram) with chip adj2 enabl\$6) and refresh\$5)	EPO; JPO;	
_	4	and clock) and reference with clock	DERWENT	2004/07/07 10:14
7	4	((((((memory or storage) and (sram or static) with	USPAT;	2004/07/07 18:14
		compatible with (dram or dynamic)) and control\$6 with	US-PGPUB;	
		(dynamic or dram) with chip adj2 enabl\$6) and refresh\$5)	EPO; JPO; DERWENT	
8	4	and clock) and reference with clock) and synchron\$7 (((((((memory or storage) and (sram or static) with	USPAT;	2004/07/07 18:15
	7	((((((Internory or storage) and (start or static) with compatible with (dram or dynamic)) and control\$6 with	US-PGPUB;	2004/07/07 18.13
		(dynamic or dram) with chip adj2 enabl\$6) and refresh\$5)	EPO; JPO;	
		and clock) and reference with clock) and synchron\$7) and	DERWENT	
		refresh\$5 with control\$5	DEIXARIAI	
9	1	i '	USPAT;	2004/07/07 18:15
	•	compatible with (dram or dynamic)) and control\$6 with	US-PGPUB;	200 1/07/07 10:15
		(dynamic or dram) with chip adj2 enabl\$6) and refresh\$5)	EPO; JPO;	
		and clock) and reference with clock) and synchron\$7) and	DERWENT	
		refresh\$5 with control\$5) and inactiva\$5 with chip adj2		
		enabl\$6		